Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-28: Currently Cancelled.

29. (Currently Amended) A method of forming a semiconductor memory cell, comprising the steps of:

forming a first region in a semiconductor substrate, wherein the substrate has a first conductivity type and the first region has a second conductivity type;

forming a trench into a surface of the semiconductor substrate, wherein the trench is spaced apart from the first region;

forming a second region in the substrate and underneath the trench, wherein the second region has the second conductivity type and a channel region in the substrate is defined between the first and second regions, the channel region includes a first portion that extends substantially along a sidewall of the trench and a second portion that extends substantially along the substrate surface;

forming a floating gate of electrically conductive material disposed over and insulated from at least a portion of the channel region and a portion of the first region; ~~[and]~~

forming a control gate of electrically conductive material having a first portion disposed in the trench; and

forming insulation material between the floating gate and the control gate that has a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

30. (Original) The method of claim 29, wherein the control gate has a second portion disposed over and insulated from the floating gate.

31. (Original) The method of claim 30, wherein the control gate forms a notch at a connection between the control gate first portion and the control gate second portion.

32. (Original) The method of claim 31, wherein the floating gate includes a sharp edge that extends toward the notch.

33. (Original) The method of claim 29, wherein the floating gate is disposed over the entire second portion of the channel region.

34. Currently Cancelled.

35. (Original) The method of claim 30, further comprising the step of:

forming a layer of insulating material that extends along sidewalls of the trench and between the control gate and the floating gate.

36. (Original) The method of claim 35, wherein the formation of the layer of insulating material includes the steps of:

forming a first portion of the layer of insulating material along sidewalls of the trench and between the control gate first portion and the channel region first portion; and

forming a second portion of the layer of insulating material under the control gate second portion and over the floating gate.

37. (Original) The method of claim 29, wherein channel region first portion extends in a direction directly toward the floating gate.

38. (Original) The method of claim 29, wherein the formation of the floating gate includes forming a layer of the electrically conductive material before the formation of the

trench, and wherein the trench is subsequently formed through a portion of the layer of electrically conductive material.

39. (Original) The method of claim 29, further including the step of:

forming an indentation in a sidewall of the trench so that the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a portion of the floating gate.

40. (Original) The method of claim 29, further including the step of:

forming an indentation in a sidewall of the trench so that the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a first part of the channel region second portion, wherein the floating gate is disposed over and insulated from a second part of the channel region second portion.

41. (Currently Amended) A method of forming an array of semiconductor memory cells, comprising the steps of:

forming a plurality of first regions in a semiconductor substrate that are substantially parallel to one another and extend in a first direction, wherein the substrate has a first conductivity type and the first regions have a second conductivity type;

forming a plurality of trenches into a surface of the semiconductor substrate, wherein the trenches are spaced apart from and extend substantially parallel to the first regions;

forming a plurality of second regions in the substrate having the second conductivity type and are substantially parallel to one another, each of the second regions extends in the first direction and is formed underneath one of the trenches, wherein a plurality of channel regions in the substrate are defined each having a first portion extending substantially along a sidewall of one of the trenches and a second portion that extends substantially along the substrate surface between the one trench and one of the first regions;

forming a plurality of floating gates of electrically conductive material each disposed over and insulated from at least a portion of one of the channel regions and a portion of one of the first regions; ~~[and]~~

forming a plurality of control gates of electrically conductive material each having a first portion disposed in one of the trenches; and

forming a layer of insulation material between each of the floating gates and one of the control gates having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

42. (Original) The method of claim 41, further comprising the steps of:

forming spaced apart isolation regions on the semiconductor substrate which are substantially parallel to one another and extend in a second direction substantially orthogonal to the first direction, with an active region between each pair of adjacent isolation regions; and

forming insulating material in portions of the trenches that are in the isolation regions.

43. (Original) The method of claim 41, wherein the control gates each have a second portion disposed over and insulated from one of the floating gates.

44. (Original) The method of claim 43, wherein for each of the active regions, the control gate second portions therein are electrically connected together.

45. (Original) The method of claim 43, wherein each of the control gates form a notch at a connection between its control gate first portion and its control gate second portion.

46. (Original) The method of claim 45, wherein each of the floating gates include a sharp edge that extends toward one of the notches.

47. (Original) The method of claim 41, wherein each of the floating gates is disposed over the entire second portion of one of the channel regions.

48. (Currently Cancelled)

49. (Original) The method of claim 43, further comprising the step of:

forming insulating material that extends along sidewalls of the trenches and between the control gates and the floating gates.

50. (Original) The method of claim 49, wherein the formation of the insulating material includes the steps of:

forming first portions of the insulating material along sidewalls of the trenches and between the control gate first portions and the channel region first portions; and

forming second portions of the insulating material under the control gate second portions and over the floating gates.

51. (Original) The method of claim 41, wherein each of the channel region first portions extends in a direction directly toward one of the floating gates.

52. (Original) The method of claim 41, wherein the formation of the floating gates includes forming a layer of the electrically conductive material before the formation of the trenches, and wherein the trenches are subsequently formed through portions of the layer of electrically conductive material.

53. (Original) The method of claim 41, further including the step of:

forming an indentation in a sidewall of each of the trenches so that the control gate first portion therein includes a protruding portion corresponding to the indentation that extends over and is insulated from a portion of one of the floating gates.

54. (Original) The method of claim 41, further including the step of:

forming an indentation in a sidewall of each of the trenches so that the control gate first portion formed therein includes a protruding portion corresponding to the indentation that extends over and is insulated from a first part of one of the channel region second portions, wherein one of the floating gates is disposed over and insulated from a second part of the one channel region second portion.